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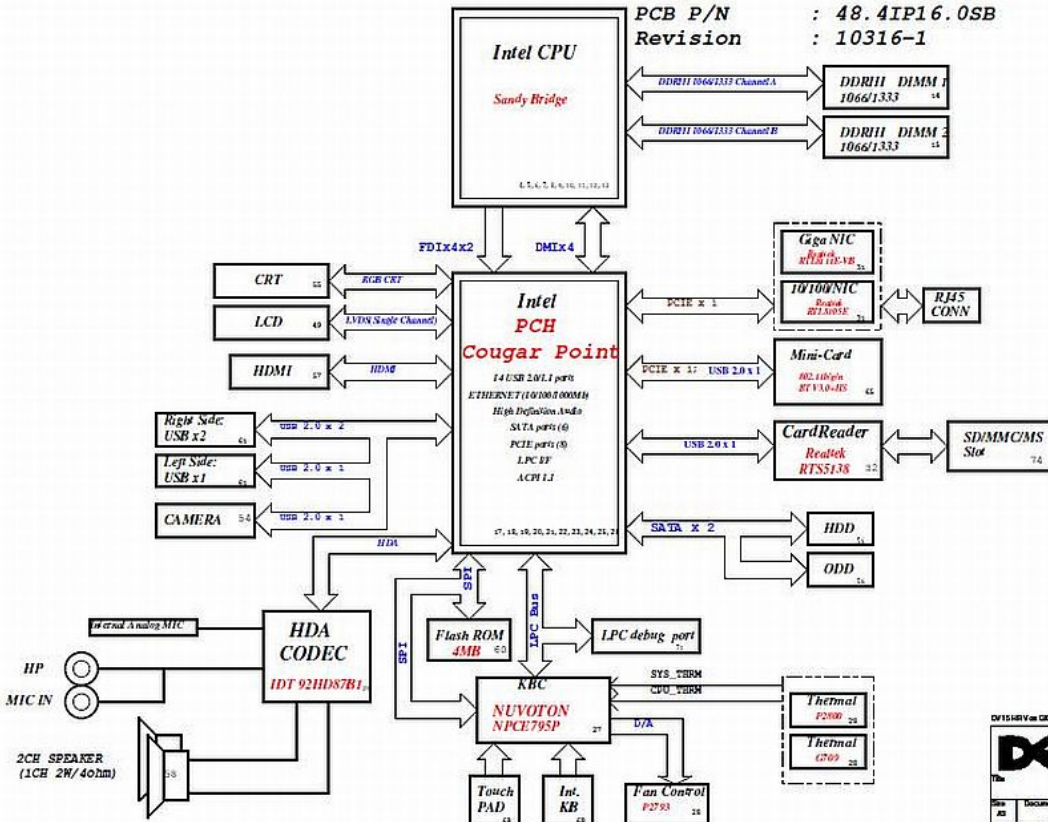


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DV15 Huron River UMA Block Diagram

Project code : 91.4IP01.001
 PCB P/N : 48.4IP16.0SB
 Revision : 10316-1



SYSTEM DC/DC TP551461 48	
INPUTS	OUTPUTS
DCIA7007	000V_50
CPU DC/DC ISL95831HRTZ 42-44	
INPUTS	OUTPUTS
DCIA7007	VCC_CORE
GFX DC/DC ISL95831HRTZ 44	
INPUTS	OUTPUTS
DCIA7007	VCC_L2P400K
SYSTEM DC/DC TP551218 45	
INPUTS	OUTPUTS
DCIA7007	100V_VFT
SYSTEM DC/DC TP551123RGER 41	
INPUTS	OUTPUTS
DCIA7007	0V_ADR_25 30V_ACR_25 0V_V_25 30V_V_25 10V_V
SYSTEM DC/DC TP551216RUKR 46	
INPUTS	OUTPUTS
DCIA7007	100V_V 001V_50 00R_VREF_50
MAXIM CHARGER BQ24707 40	
INPUTS	OUTPUTS
DCIA7007	0V_IC_25 +PGAT
SYSTEM DC/DC TP551311RGR 47	
INPUTS	OUTPUTS
DCIA7007	30V_55 100V_50
Switches	
INPUTS	OUTPUTS
DCIA7007	100V_50 0V_50 30V_50 30V_50
PCB LAYER	
L1: Top	L4: Signal
L2: CND	L5: VCC
L3: Signal	L6: Bottom

DV15 HEV Via CECA HDMI NoCharge

Wistron Corporation
 21F, 22, Sec. 1, Hsin Tai Wu Rd., Hsuehshui, Taipei 106, Taiwan, R.O.C.

The Block Diagram

Rev: 03	DocuMent Number: Erica/Caruso 15 HR	Rev: 03
Date: Thursday, June 02, 2010	Sheet: 2	of: 09

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